Docket No.: H1840 ***PATENT***

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Errol Todd Ryan et al.	: Confirmation No.:	2466
Serial No.:	10/791,096	: Art Unit:	2813
Filed:	3/1/2004	: Examiner:	Heather Anne Doty
For:	CONTACT LINER IN INTEGRATED CIRCUIT TECHNOLOGY	:	

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Sir/Madam:

The following Appeal Brief is submitted pursuant to the Notice of Appeal filed March 11, 2006 in the above-identified Application.

TABLE OF CONTENTS

(1) Real party in interest

The real party in interest is Advanced Micro Devices, Inc., having its principal place of business in Sunnyvale, CA.

(2) ***Related appeals and interferences*** [LOMI 121]

There are no known related appeal or interference cases.

(3) Status of claims [LOMI 122]

Claims 1-2, 4-7, 9-12, 14-17, 19 and 20, the only claims pending, stand under final rejection, from which rejection this Appeal is taken.

(4) Status of amendments [LOMI 123]

No amendments have been filed subsequent to the final rejection of December 13, 2005.

(5) Summary of claimed subject matter

1. A method of forming an integrated circuit comprising:

providing a semiconductor substrate [102; p. 5, lns. 18-22];

forming a gate dielectric [104; p. 5, lns. 18-22] on the semiconductor substrate [102; p. 5, lns. 18-22];

forming a gate [106; p. 5, lns. 18-22] on the gate dielectric [104; p. 5, lns. 18-22];

forming source/drain junctions [304, 306; p. 5, ln. 29-p. 6, ln. 2; 504,506; p. 6, lns. 8-9] in the semiconductor substrate [102; p. 5, lns. 18-22];

forming a silicide [604, 606, 608; p. 6, lns.16-24] on the source/drain junctions [304, 306; p. 5, ln. 29-p. 6, ln. 2; 504,506; p. 6, lns. 8-9] and on the gate [106; p. 5, lns. 18-22] within a thermal budget having a temperature dependent upon a silicide metal;

depositing an interlayer dielectric [702; p. 8, lns. 3-5] having contact holes therein above the semiconductor substrate [102; p. 5, lns. 18-22];

forming contact liners [801, 803, 805; p. 8, lns. 18-22] in the contact holes within the thermal budget for forming the silicide [604, 606, 608; p. 6, lns.16-24]; and

forming contacts [802, 804, 806; p. 8, lns. 19-20] in the contact holes over the contact liners [801, 803, 805; p. 8, lns. 18-22], whereby the contact liners [801, 803, 805; p. 8, lns. 18-22] are formed of a nitride of the material of the contacts [802, 804, 806; p. 8, lns. 19-20].

6. A method of forming an integrated circuit comprising:

providing a semiconductor substrate [102; p. 5, lns. 18-22];

forming a gate dielectric [104; p. 5, lns. 18-22] on the semiconductor substrate [102; p. 5, lns. 18-22];

forming a gate [106; p. 5, lns. 18-22] on the gate dielectric [104; p. 5, lns. 18-22];

forming source/drain junctions [304, 306; p. 5, ln. 29-p. 6, ln. 2; 504,506; p. 6, lns. 8-9] in the semiconductor substrate [102; p. 5, lns. 18-22];

forming a nickel silicide [604, 606, 608; p. 6, lns.16-24] on the source/drain junctions [304, 306; p. 5, ln. 29-p. 6, ln. 2; 504,506; p. 6, lns. 8-9] and on the gate [106; p. 5, lns. 18-22] within a thermal budget having a temperature of less than about 400 degrees centigrade;

depositing an interlayer dielectric [702; p. 8, lns. 3-5] having contact holes therein above the semiconductor substrate [102; p. 5, lns. 18-22];

forming tungsten nitride contact liners [801, 803, 805; p. 8, lns. 18-22] in the contact holes within the thermal budget for forming the nickel silicide [604, 606, 608; p. 6, lns.16-24]; and

forming tungsten contacts [802, 804, 806; p. 8, lns. 19-20] in the contact holes over the contact liners [801, 803, 805; p. 8, lns. 18-22].

9. The method as claimed in claim 6 wherein:

forming the nickel silicide [604, 606, 608; p. 6, lns.16-24] uses an ultra-thin thickness of a nickel silicide metal.

11. An integrated circuit comprising:

a semiconductor substrate [102; p. 5, lns. 18-22];

a gate dielectric [104; p. 5, lns. 18-22] on the semiconductor substrate [102; p. 5, lns. 18-22];

a gate [106; p. 5, lns. 18-22] on the gate dielectric [104; p. 5, lns. 18-22];

source/drain junctions [304, 306; p. 5, ln. 29-p. 6, ln. 2; 504,506; p. 6, lns. 8-9] in the semiconductor substrate [102; p. 5, lns. 18-22];

an ultra-thin silicide [604, 606, 608; p. 6, lns.16-24] on the source/drain junctions [304, 306; p. 5, ln. 29-p. 6, ln. 2; 504,506; p. 6, lns. 8-9] and on the gate [106; p. 5, lns. 18-22];

an interlayer dielectric [702; p. 8, lns. 3-5] having contact holes therein above the semiconductor substrate [102; p. 5, lns. 18-22];

contact liners [801, 803, 805; p. 8, lns. 18-22] in the contact holes; and

contacts [802, 804, 806; p. 8, lns. 19-20] in the contact holes over the contact liners [801, 803, 805; p. 8, lns. 18-22], whereby the contact liners [801, 803, 805; p. 8, lns. 18-22] are formed of a nitride of the material of the contacts [802, 804, 806; p. 8, lns. 19-20].

17. An integrated circuit comprising:

a semiconductor substrate [102; p. 5, lns. 18-22];

a gate dielectric [104; p. 5, lns. 18-22] on the semiconductor substrate [102; p. 5, lns. 18-22];

a gate [106; p. 5, lns. 18-22] on the gate dielectric [104; p. 5, lns. 18-22];

source/drain junctions [304, 306; p. 5, ln. 29-p. 6, ln. 2; 504,506; p. 6, lns. 8-9] in the semiconductor substrate [102; p. 5, lns. 18-22];

an ultra-thin thickness of a nickel silicide [604, 606, 608; p. 6, lns.16-24] on the source/drain junctions [304, 306; p. 5, ln. 29-p. 6, ln. 2; 504,506; p. 6, lns. 8-9] and on the gate [106; p. 5, lns. 18-22],

an interlayer dielectric [702; p. 8, lns. 3-5] having contact holes therein above the semiconductor substrate [102; p. 5, lns. 18-22];

tungsten nitride contact liners [801, 803, 805; p. 8, lns. 18-22] in the contact holes; and

tungsten contacts [802, 804, 806; p. 8, lns. 19-20] in the contact holes over the contact liners [801, 803, 805; p. 8, lns. 18-22].

(6) Grounds for Rejection to be reviewed on appeal [LOMI 124]

Issue #1:

Claims 1-8, 11, 12, 15-17, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. Patent 6,858,506, hereinafter "Chang") in view of Lim (U.S. 2004/0115929, hereinafter "Lim").

Issue #2:

Claims 9, 13, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. 6,858,506, hereinafter "Chang") in view of Lim (U.S. 2004/0115929, hereinafter "Lim") as applied to claims 6, 11, and 17 above, and further in view of Tseng (U.S. 2005/0035460, hereinafter "Tseng").

(7) Arguments[LOMI 125]

Issue #1:

Claims 1-8, 11, 12, 15-17, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. Patent 6,858,506, hereinafter "Chang") in view of Lim (U.S. 2004/0115929, hereinafter "Lim").

Chang teaches a metal oxide transistor having a strained channel by forming a SiGe layer on the surface of a substrate and then forming a strained silicon layer over the SiGe layer. Chang does not teach or suggest the formation of an interlayer dielectric layer having contact holes formed therein, the formation of contact liners, or the formation of contacts.

Lim teaches a method of manufacturing a semiconductor device by forming a tungsten nitride layer in contact holes using an atomic layer deposition method. There is no teaching or suggestion of the formation of a silicide or a thermal budget for the formation of a silicide.

Claims 1, 6, 11, and 17 includes limitations, as exemplified in claim 1, not taught or suggested by Chang or Lim, taken either singly or in combination, of:

> "forming a silicide on the source/drain junctions and on the gate within a thermal budget having a temperature dependent upon the silicide metal;
>
> forming contact liners in the contact holes within the thermal budget for forming the silicide"

The Examiner stated:

> "Chang teaches ... forming a nickel silicide on the source/drain junctions and on the gate (234 in Fig. 2G; column 4, line 56 - column 5, line 10)."

Thus, Chang does not teach, suggest, or mention the claimed thermal budget as indicated in Chang col. 4, line 56-col. 5, line 10, which states:

> "Referring to FIG. 2G, ... A silicide film 234 is formed atop the gate structure 208a and the heavily doped source/drain regions 218 to lower the sheet resistance at the source/drain area and the gate electrode. In the case a nickel silicide is formed, the consumption of silicon in the gate structure 208a

> and the strained silicon layer 204 can also be reduced. ...a very low sheet resistance silicide, constructed with silicon germanium, can also be formed in the source/drain area." [deletions for clarity]

However, Chang states that the Chang silicide is subject to a high temperature anneal in Chang col. 4, lines 62-64:

> "After executing an annealing process, for example, at a temperature of about 400 to 800 degrees Celsius for about 20 to 60 seconds..."

The thermal budget is the cummulative number of degrees of temperature that an integrated circuit can be subjected to during its various manufacturing processes before excess dopant migration occurs and an integrated circuit will no longer function properly. As integrated circuits have been reduced in size, the thermal budget has also been reduced. By teaching a high range of post-siliciding anneal, Chang indicates that the thermal budget of the Chang silicide is not critical and therefore teaches away from Appellants' invention as claimed.

The Chang teaching away is even clearer because the claim limitations require both the silicide and the contact liners to be formed within the thermal budget for forming the silicide alone.

The Examiner also has stated:

> "Chang does not teach depositing an interlayer dielectric having contact holes therein above the semiconductor substrate; forming contact liners in the contact holes; and forming contacts in the contact holes over the contact liners, whereby the contact liners are formed of a nitride of the material of the contacts."

Appellants agree that Chang fails to teach the formation of an interlayer dielectric layer, any contact holes in the interlayer dielectric, any contact liners of any type in the contact holes, much less at the thermal budget claimed by Appellants. Appellants respectfully submit that Chang teaches away from Appellants' invention.

The Examiner also has stated:

> "Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the teachings of Chang by additionally depositing an interlayer dielectric having contact holes therein above the semiconductor substrate; forming contact liners in the contact holes; and forming contacts in the contact holes over the contact liners, whereby the contact liners are formed of tungsten nitride and the contacts are formed of

> tungsten, as taught by Lim. The motivation for doing so at the time of the invention would have been that the method taught by Lim simplifies a deposition process of a tungsten nitride layer as a barrier metal, as expressly taught by Lim (paragraph 0014)."

However, Lim does not teach, suggest, or even mention the formation of any silicide much less within the thermal budget claimed by Appellants. Accordingly, it is respectfully submitted that Lim fails to teach or suggest Appellants' invention as claimed in independent claim 1.

Appellants respectfully submit that the combination of references do not even mention all the claim limitations:

> "[T]he prior art reference (or references when combined) must teach or suggest **all** the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re* Vaeck, 947 F2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) [bold for clarity]

Further because the references as a whole teach away from each other as previously explained above, the combination cannot be obvious according to the CAFC:

> "We have noted elsewhere, as a "useful general rule," that references that teach away cannot serve to create a prima facie case of obviousness...", we have held that such references teach away from the combination and thus cannot serve as predicates for a prima facia case of obviousness." *In re* Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984)[underlining and for clarity]

With regard to claims 2 and 4-5, claims 2 and 4-5, depend upon claim 1 and are believed to be allowable for the reasons set forth above with regard to claim 1 since they contain all the limitations set forth in the independent claim from which they depend and claim non-obvious combinations thereof because of *In re* Vaeck, *supra* and *In re* Gordon, *supra.*

With regard to claim 6, claim 6 includes the limitations not taught or suggested by Chang or Lim, taken either singly or in combination, of:

> "forming a nickel silicide on the source/drain junctions and on the gate within a thermal budget having a temperature of less than about 400 degrees centigrade;

forming tungsten nitride contact liners in the contact holes within the thermal budget for forming the nickel silicide"

The Examiner has stated:

"Regarding claims 6 and 17, Chang teaches a method of forming an integrated circuit comprising providing a semiconductor substrate (200 in Fig. 2D); forming a gate dielectric on the semiconductor substrate (206 in Fig. 2D; column 3, lines 36-39); forming a gate on the gate dielectric (208 in Fig. 2D; column 3, lines 46-47); forming source/drain junctions in the semiconductor substrate (210 in Fig. 2D; column 3, line 59-column 4, line 39); and forming a nickel silicide on the source/drain junctions and on the gate (234 in Fig. 2G; column 4, line 56 - column 5, line 10)."

However, Chang states with respect to formation of the Chang silicide at column 4, lines 62-64:

"After executing an annealing process, for example, at a temperature of about 400 to 800 degrees Celsius for about 20 to 60 seconds..."

Chang therefore teaches formation of a silicide having a temperature higher than that claimed by Appellants, and consequently teaches away from Appellants' invention.

The Examiner also stated:

"Chang does not teach depositing an interlayer dielectric having contact holes therein above the semiconductor substrate; forming tungsten nitride contact liners in the contact holes; and forming tungsten contacts in the contact holes over the contact liners."

Appellants agree that Chang fails to teach the formation of an interlayer dielectric layer, any contact holes in the interlayer dielectric, any contact liners of any type in the contact holes, much less at the thermal budget claimed by Appellants. Appellants respectfully submit that Chang teaches away from Appellants' invention.

The Examiner also has stated:

"Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the teachings of Chang by additionally depositing an interlayer dielectric having contact holes therein above the semiconductor substrate; forming tungsten nitride contact liners in the contact holes; and forming tungsten contacts in the contact holes over the contact liners, as taught by Lim. The motivation for doing so at the time of the invention would have been that the method taught by Lim simplifies a deposition process of a tungsten nitride layer as a barrier metal, as expressly taught by Lim (paragraph 0014)."

However, Lim does not teach, suggest, or even mention the formation of any silicide much less within the thermal budget claimed by Appellants. Accordingly, it is respectfully submitted that Lim fails to teach or suggest Appellants' invention as claimed in independent claim 1.

Appellants respectfully submit that claim 6 is allowable over Chang in view of Lim taken either singly or in combination because of *In re* Vaeck, *supra* and *In re* Gordon, *supra.*

With regard to claim 7, claim 7 depends upon claim 6 and is believed to be allowable for the reasons set forth above with regard to claim 6 since it contains all the limitations set forth in the independent claim from which it depends and claims non-obvious combinations thereof because of *In re* Vaeck, *supra* and *In re* Gordon, *supra.*

With regard to claim 11, claim 11 includes the limitation not taught or suggested by Chang or Lim, taken either singly or in combination, of:

> "an ultra-thin silicide on the source/drain junctions and on the gate"

With respect to claim 11, the Examiner has stated the same rejection with regard to claim 1 above.

However, Chang is silent with respect to the thickness of the silicide (see for example, column 4, lines 56-67). Also as stated above Lim does not teach, suggest, or even mention the formation of any silicide much less an ultra-thin silicide as claimed by Appellants.

Accordingly, Appellants submit that claim 11 is allowable over Chang in view of Lim taken either singly or in combination because of *In re* Vaeck, supra and *In re* Gordon, supra.

With regard to claims 12, 15, and 16, claims 12, 15, and 16 depend upon claim 11 and are believed to be allowable for the reasons set forth above with regard to claim 11 since they contain all the limitations set forth in the independent claim from which they depend and

claim non-obvious combinations thereof because of *In re* Vaeck, *supra* and *In re* Gordon, *supra*.

With regard to claim 17, claim 17 has been clarified to include the limitation not taught or suggested by Chang or Lim, taken either singly or in combination, of:

> "an ultra-thin thickness of a nickel silicide on the source/drain junctions and on the gate"

With respect to claim 17, the Examiner has stated the same rejection with regard to claim 6 above.

However, Chang does not teach, suggest, or mention the thickness of the silicide (see for example, column 4, lines 56-67). Also as stated above Lim does not teach, suggest, or mention the formation of any silicide much less an ultra-thin silicide as claimed by Appellants.

Accordingly, Appellants submit that claim 17 is allowable over Chang in view of Lim taken either singly or in combination because of *In re* Vaeck, *supra* and *In re* Gordon, *supra*.

With regard to claim 20, claim 20 depends upon claim 17 and is believed to be allowable for the reasons set forth above with regard to claim 17 since it contains all the limitations set forth in the independent claim from which it depends and claims non-obvious combinations thereof because of *In re* Vaeck, *supra* and *In re* Gordon, *supra*.

Issue #2:

Claims 9, 13, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. 6,858,506, hereinafter "Chang") in view of Lim (U.S. 2004/0115929, hereinafter "Lim") as applied to claims 6, 11, and 17 above, and further in view of Tseng (U.S. 2005/0035460, hereinafter "Tseng").

With regard to claims 9, 13, and 18, claim 9 depends respectively upon independent claims 6 and is believed to be allowable for the reasons set forth above with regard to claim 6, since it contains all the limitations set forth in the independent claim from

which it depends and claims non-obvious combinations thereof because of *In re* Vaeck, *supra* and *In re* Gordon, *supra.* Claims 13 and 18 have been cancelled and rewritten as respective independent claims 11 and 17.

Further with regard to these claims, the Examiner has stated:

> "Regarding claims 9, 13, and 18, Chang and Lim together teach the method of claim 6 and the device of claims 11 and 17 (note 35 U.S.C. 103(a) rejections above). They do not teach that forming the nickel silicide uses an ultra-thin thickness of a nickel silicide.

Appellants agree that Chang and Lim, taken either singly or in combination, fail to teach or suggest forming an ultra-thin nickel silicide.

The Examiner also stated:

> "Tseng teaches forming nickel silicide layers with a thickness of 50 - 350 Å (paragraph 0037), within the limits indicated in the instant specification on page 8, line 4 of "not more than 50 Å thickness."

However, Tseng specifically states at paragraph [0037]:

> "The metal silicides ... preferably have a thickness between about 50 Å and 350 Å." [deletions and underlining for clarity]

Appellants submit that the teaching of silicides having a thickness greater than the claimed thickness actually teaches away from Appellants' invention.

Assuming *arguendo* that "not more than 50 Å" and "between about 50 Å and 350 Å" is considered an overlap in range, the C.C.P.A. has held that:

> "ranges which overlap or lie inside ranges disclosed by the prior art may be patentable if the applicant can show criticality in the claimed range by evidence of unexpected results." (*In re Wertheim*, 541 F.2d 257, 191 USPQ 90 (C.C.P.A. 1976) at 100 (citing *In re Malagari*, 499 F.2d 1297, 182 USPQ 549 (C.C.P.A. 1974); *In re Orfeo*, 440 F.2d 439, 169 USPQ 487 (C.C.P.A. 1971)).

Appellants have shown criticality on page 7, lines 17-33:

> "While the present invention may be used with various refractory metal silicides, it has been found that nickel silicide has many desirable characteristics. However, in working with nickel silicide, it has been found to be difficult to form robust nickel. It has been thought that thick silicides around 100 Å thick with rough surfaces would best protect the silicon substrate and provide good adhesion.
>
> However, an ultra-uniform nickel silicide can form extremely robust nickel silicide. By definition, an ultra-uniform silicide means a layer of

> silicide where there are no variations in thickness greater than about 3% of the overall thickness.
>
> ...
>
> Still further, it is preferable that the silicide be deposited under these power levels and deposition rates to an ultra-thin thickness of not more than 50 Å thickness in order to provide an ultra-uniform, ultra-thin silicide.

Accordingly, Appellants submit that the Examiner's proposed combination of Chang, Lim and Tseng is improper because of *In re* Vaeck, *supra* and *In re* Gordon, *supra.*

Allowance of claims 9, 11, and 17 is hereby solicited.

(8) Claims Appendix

See Appendix I[LOMI 126]

(9) EvidenceAappendix

See Appendix II

[LOMI 127]

(10) Related Proceedings Appendix

See Appendix III[LOMI 128]

Conclusion and Relief Requested:

Claims 1-2, 4-7, 9-12, 14-17, 19, and 20 are patentable over the prior art.

Reversal of the Examiner's decision is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including any extension of time fees, to Deposit Account No. 50-0374 and please credit any excess fees to such deposit account.

Respectfully submitted,

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APPENDICES follow on separate pages

(8) Claims appendix

Appendix I – Claims on Appeal

1. A method of forming an integrated circuit comprising:

providing a semiconductor substrate;

forming a gate dielectric on the semiconductor substrate;

forming a gate on the gate dielectric;

forming source/drain junctions in the semiconductor substrate;

forming a silicide on the source/drain junctions and on the gate within a thermal budget having a temperature dependent upon a silicide metal;

depositing an interlayer dielectric having contact holes therein above the semiconductor substrate;

forming contact liners in the contact holes within the thermal budget for forming the silicide; and

forming contacts in the contact holes over the contact liners, whereby the contact liners are formed of a nitride of the material of the contacts.

2. The method as claimed in claim 1 wherein:

forming the contact liners uses an atomic layer deposition process.

4. The method as claimed in claim 1 wherein:

forming the silicide forms a nickel silicide.

5. The method as claimed in claim 1 wherein:

forming the contacts forms a tungsten material; and

forming the contact liners forms a tungsten nitride material.

6. A method of forming an integrated circuit comprising:

providing a semiconductor substrate;

forming a gate dielectric on the semiconductor substrate;

forming a gate on the gate dielectric;

forming source/drain junctions in the semiconductor substrate;

forming a nickel silicide on the source/drain junctions and on the gate within a thermal budget having a temperature of less than about 400 degrees centigrade;

depositing an interlayer dielectric having contact holes therein above the semiconductor substrate;

forming tungsten nitride contact liners in the contact holes within the thermal budget for forming the nickel silicide; and

forming tungsten contacts in the contact holes over the contact liners.

7. The method as claimed in claim 6 wherein:

forming the tungsten nitride contact liners uses an atomic layer deposition process.

9. The method as claimed in claim 6 wherein:

forming the nickel silicide uses an ultra-thin thickness of a nickel silicide metal.

10. The method as claimed in claim 6 wherein:

depositing the interlayer dielectric deposits a dielectric material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants.

11. An integrated circuit comprising:

a semiconductor substrate;

a gate dielectric on the semiconductor substrate;

a gate on the gate dielectric;

source/drain junctions in the semiconductor substrate;

an ultra-thin silicide on the source/drain junctions and on the gate;

an interlayer dielectric having contact holes therein above the semiconductor substrate;

contact liners in the contact holes; and

contacts in the contact holes over the contact liners, whereby the contact liners are formed of a nitride of the material of the contacts.

12. The integrated circuit as claimed in claim 11 wherein:

the silicide is a nickel silicide.

14. The integrated circuit as claimed in claim 11 wherein:

the interlayer dielectric is a dielectric material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants.

15. The integrated circuit as claimed in claim 11 wherein:

the contacts in the contact holes are materials selected from a group consisting of tantalum, titanium, tungsten, copper, gold, silver, an alloy thereof, a compound thereof, and a combination thereof.

16. The integrated circuit as claimed in claim 11 wherein:

the contacts are a tungsten material; and

the contact liners are a tungsten nitride material.

17. An integrated circuit comprising:

a semiconductor substrate;

a gate dielectric on the semiconductor substrate;

a gate on the gate dielectric;

source/drain junctions in the semiconductor substrate;

an ultra-thin thickness of a nickel silicide on the source/drain junctions and on the gate,

an interlayer dielectric having contact holes therein above the semiconductor substrate;

tungsten nitride contact liners in the contact holes; and

tungsten contacts in the contact holes over the contact liners.

19. The integrated circuit as claimed in claim 17 wherein:

the interlayer dielectric is a dielectric material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants.

20. The integrated circuit as claimed in claim 17 wherein:

the nickel silicide further comprises arsenic doping.

(9) Evidence appendix

Appendix *II* [LOMI 129]

Evidence under 37 CFR 1.130, 1.131, or 1.132 entered by examiner and relied upon by appellant or any other evidence entered by the examiner and relied upon by appellant in the appeal, along with a statement setting forth where in the record that evidence was entered by the examiner

(37 CFR 41.37(c)(1)(ix)

None

(10) Related Proceedings appendix

APPENDIX III[LOMI 1210]

Decisions rendered by a court or the Board identified in Related Appeals and Interferences section

(37 CFR 41.37(c)(1)(x)

Copies of the following decisions are herein enclosed:

None